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NOTICE OF ALLOWANCE AND FEE(S) DUE

95671 7590 10/04/2011

Synopsys/Fenwick
Silicon Valley Center
801 California Street
Mountain View, CA 94041

EXAMINER
SOWARD, IDA M

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/04/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,037	09/12/2003	John D. Hyde	22524-17802	6704

TITLE OF INVENTION: APPARATUS FOR TRIMMING HIGH-RESOLUTION DIGITAL-TO-ANALOG CONVERTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$0	$0	$1740	01/04/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

95671 7590 10/04/2011

Synopsys/Fenwick
Silicon Valley Center
801 California Street
Mountain View, CA 94041

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,037	09/12/2003	John D. Hyde	22524-17802	6704

TITLE OF INVENTION: APPARATUS FOR TRIMMING HIGH-RESOLUTION DIGITAL-TO-ANALOG CONVERTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$0	$0	$1740	01/04/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOWARD, IDA M	2822	257-316000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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10/661,037	09/12/2003	John D. Hyde	22524-17802	6704

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/04/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 979 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 979 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	10/661,037	HYDE ET AL.	
	Examiner	Art Unit	
	IDA M. SOWARD	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Applicants' amendment filed July 28, 2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *36,39,40,44-48 and 51-63*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/IDA M SOWARD/
Primary Examiner, Art Unit 2822

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed July 28, 2011.

Specification

The objection to the title of the invention has been withdrawn due to the amendment filed.

Claim Objections

The objection to claims 46 and 48 has been withdrawn due to the amendment filed.

Claim Rejections - 35 USC § 112

The objection to claims 36, 44, 45, 46, 47 and 48 under 35 U.S.C. 112, second paragraph, has been withdrawn due to the amendment filed.

Allowable Subject Matter

Claims 36, 39-40, 44-48 and 51-63 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as:

In claim 36, "a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased when a voltage difference between the first source and the first drain is increased; and a channel disposed in said first n- well between said source and said drain; a first layer of gate oxide above said channel and said first n- well; and a first polysilicon floating gate disposed above said layer of gate oxide; and a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising: a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region; a second layer of gate oxide above said first n- well; a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased when voltage at the second drain or the second source is increased, wherein the conductor comprises a conductive laver which forms a bridge over said second polysilicon floating gate";

In claim 44, "a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased responsive to

increase in when a voltage difference between the first source and the first drain is increased; and a channel disposed in said first n- well between said source and said drain; a first layer of gate oxide above said channel and said first n- well; and a first polysilicon floating gate disposed above said layer of gate oxide; and a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising: a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region; a second layer of gate oxide above said first n-well; a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased when voltage at the second drain or the second source is increased, wherein the conductor comprises a conductive layer which forma s bridge over said second polysilicon floating gate; and a well contact terminal electrically coupled to said second n- well, wherein said synapse transistor is configured to operate as a current source without gate input using a single polysilicon gate layer";

In claim 45, "a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased when a voltage difference between the first source and the first drain is increased; and a channel disposed in said first n- well between said source and said drain; a first layer of gate

oxide above said channel and said first n- well; and a first polysilicon floating gate disposed above said layer of gate oxide; and a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising: a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region; a second layer of gate oxide above said first n- well; a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased when voltage at the second drain or the second source is increased";

In claim 46, "a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased when a voltage difference between the first source and the first drain is increased; and a channel disposed in said first n- well between said source and said drain; a first layer of gate oxide above said channel and said first n- well; and a first polysilicon floating gate disposed above said layer of gate oxide; and a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising: a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region; a

second layer of gate oxide above said first n- well; a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and a conductor connecting the second drain and the second source, a number of electrons removed from the second polysilicon floating gate is increased when voltage at the second drain or the second source is increased";

In claim 47, "a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased when a voltage difference between the first source and the first drain is increased; and a channel disposed in said first n- well between said source and said drain; a first layer of gate oxide above said channel and said first n- well; and a first polysilicon floating gate disposed above said layer of gate oxide; and a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising: a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region; a second layer of gate oxide above said first n- well; a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased when voltage at the second drain or the second source is increased"; and

In claim 48, “a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate is increased when a voltage difference between the first source and the first drain is increased; and a channel disposed in said first n- well between said source and said drain; a first layer of gate oxide above said channel and said first n- well; and a first polysilicon floating gate disposed above said layer of gate oxide; and a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising: a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well, wherein the second drain comprises a third p+ doped region within the second n-well, and the second source comprises a fourth p+ doped region; a second layer of gate oxide above said first n- well; a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and a conductor connecting the second drain and the second source, wherein a number of electrons removed from the second polysilicon floating gate is increased when voltage at the second drain or the second source is increased”.

The dependent claims being further limiting and definite are also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to transistor devices:

Awaka et al. (US 6,307,233 B1)

Chishiki (5,714,796)

Fujita et al. (5,336,915)

Jeon (5,373,476)

Kimura et al. (5,323,043)

Kumagai (US 6,329,693 B1)

Miyazaki (5,537,075)

Ouchi et al. (6,097,067).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS
September 28, 2011
/Ida M Soward/
Primary Examiner, Art Unit 2822